# Lattice Wireframes

CONFIDENTIAL DOCUMENT

| Version Release History | Disclaimer: Wireframes represent information structure, general page level functionality and user interface/navigation component hierarchy only. They do not represent final copy, visual layout, graphic design or typography. |
| --- | --- |

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Lattice Wifeframes

Wireframes 3.0
Wed Dec 26 2012

Wireframe Page: Document Version & Legend

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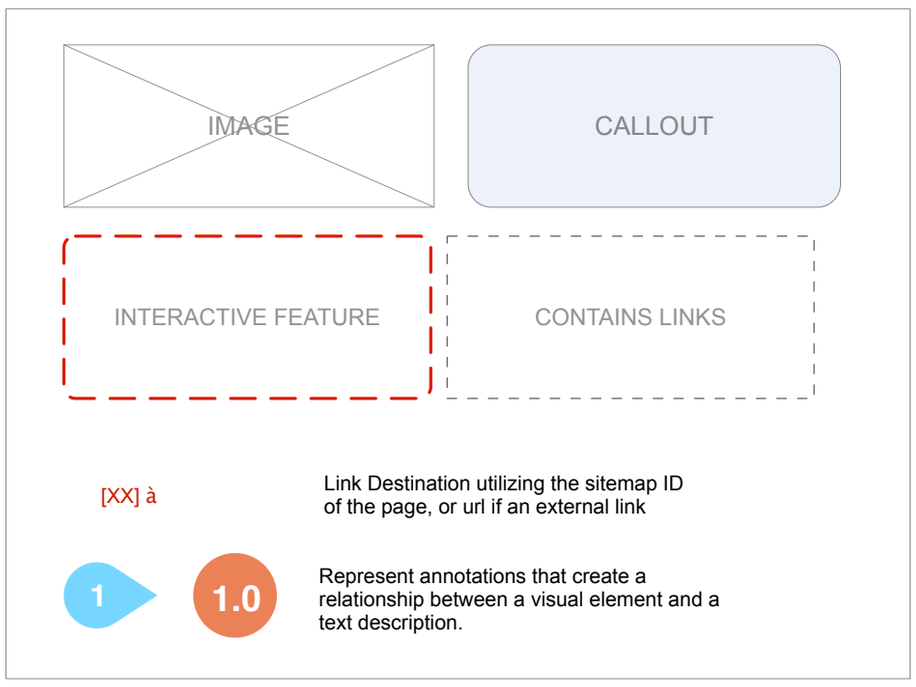
VERSION

| DATE | VERSION | MODIFIED BY | MODIFICATIONS |
|---|---|---|---|
| Wed Dec 26 2012 | 1.0 | Chava Alexander | Initial Rough Draft |

## LEGEND




## ABOUT THIS DOCUMENT

### What is a Wireframe?

Wireframes are a page blueprint prior to the visual design used to illustrate the flow of information, document all objects to be included on the page, and show the behavior and states of some of these objects. They are not meant to reflect actual design or content.

### Design Aspects for Consideration:

- Representation of selected content and functionality that will reside on a page to bring the strategic concept to life.
- An allocation of page real estate to illustrate priority and placement.
- Intent of copy - indicative of the eventual design. This includes titles, labels, links, prompts, and instructions.
- Schematic that identifies key page areas (modules).
- Direction for visual design explorations.

### Aspects Not for Wireframe Review:

- Final copy or branding treatments
- The design/look · &· feel of the page
- Representation of the specific photography to be used
- The final layout of future content and functionality·

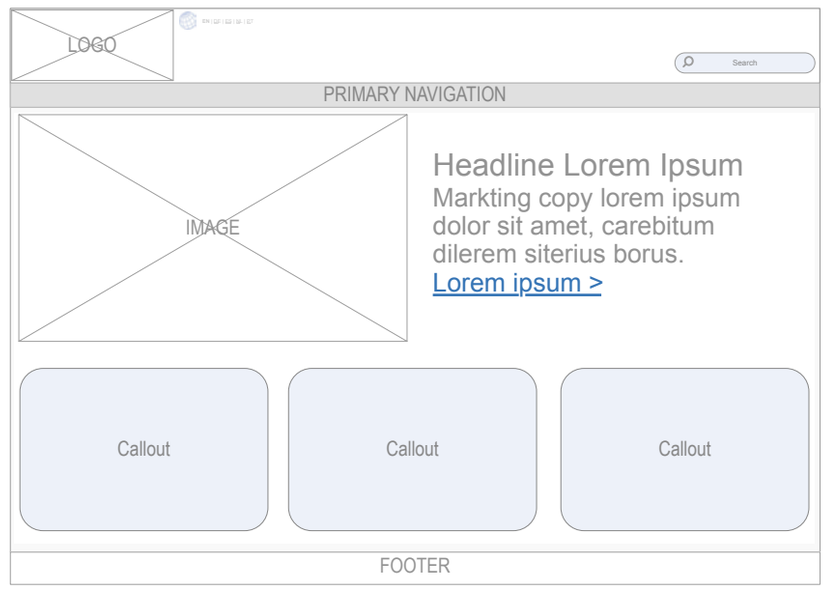
### CTA:

- All CTA's throughout the document are internal advertisements

### Key Contacts:

·Maximum of two contacts unless otherwise noted

## WIREFRAME EXAMPLE



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Callout: Carousel #1 | Callout: Carousel #2 | Callout: Carousel #3 | Callout: Carousel #4

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1. When the user is signed in, there name will appear here (ex. "Welcome, John Doe"

Lattice Wifeframes

Wireframes 3.0
Wed Dec 26 2012

Wireframe Page: Homepage (0.0) (Products)

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Product Image

FPGA & CPLD Devices

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- Lattice ECP3
- Lattice ECP2M
- Lattice SC/M
- Lattice XP2
- MachXO2
- MachXO
- ICE40
- ISPMach4000ZE

Product Family Selector Image

Product Image

Power and Clock Devices

Lorem ipsum dolor sit amet, consectetuer adipiscing elit.

- Platform Manager
- Power Manager II
- Clock Devices

Design Software and Intellectual Property

- Lattice Diamond
- IceCube2
- ISPLever Classic
- LatticeMICO System
- ISPVM System
- IP Core Library
- ORCAstra
- PAC-Designer
- ISPLever Software
- Reference Designs
- Software Archive
- Licensing

Development Kits and Boards

- All Boards and Kits
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### Technology Solutions

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- PCI Express
- Ethernet
- Memory Interfaces

### Market Solutions

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- Wireless
- Industrial
- Consumer
- Automotive
- Video and Display
- Wireline
- Security and Survielance

### Partner Solutions

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- Texas Instruments

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Recently Updated
Prerelease Flag

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- Other
- Other
- View All

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Enter Part Number

Not Sure? Part Number Help

- Silicon Devices
- Software Cable and Boards

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FPGA University
- What is an FPGA Device?
- What is Verilog?
- What is Place and Route?
- How do I get started?

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- Low Cost
- Devices
- History

Case Studies

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- Reps

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### My Support Liaison

[First Name Last Name]
Lattice Support Liaison
[email address]
[phone number]

[First Name] is online. Chat Now

Photo of Support Liaison

### How Can We Help You?

Image | Image | Image | Image

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### Power and Clock Devices

Product Image

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### Design Software and Intellectual Property

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### Development Boards and Kits

Product Image

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Product Image

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| | [Function] | [Product] | [Vendor] |

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Product Image

# [Solution Name]

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## Solutions

- Technology Solutions
  - PCI Express
  - Ethernet
  - Memory Interfaces
- Market
- Partner

## Most Popular

- Lorem Ipsum
- Lorem Ipsum
- Lorem Ipsum
- Lorem Ipsum
- Lorem Ipsum

Product Family Selector Image

**Block Diagram** | Features | IP | **Development Kits, Boards and Demos** | Documentation

## Development Kits, Boards and Demos

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### Device Family  Product Name  Accessories

| | | |
|---|---|---|
| [Family Name] | [Protocol Name] | [Accessories] |
| | [Protocol Name] | [Accessories] |
| | [Protocol Name] | [Accessories] |

| | | |
|---|---|---|
| [Family Name] | [Protocol Name] | [Accessories] |
| | [Protocol Name] | [Accessories] |
| | [Protocol Name] | [Accessories] |

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# [Solution Name]

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## Solutions

- Technology Solutions
  - PCI Express
  - Ethernet
  - Memory Interfaces
- Market
- Partner

## Most Popular

- Lorem Ipsum
- Lorem Ipsum
- Lorem Ipsum
- Lorem Ipsum
- Lorem Ipsum

Product Family Selector Image

**Block Diagram** | Features | IP | Development Kits, Boards and Demos | **Documentation**

## Documentation

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## Support

- Technical Support
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- Training
- What's New
- Design Services
- Quality and Reliability
- Mature and Discontinued Devices

## Answer Database

- Lorem Ipsum

## Submit a Ticket

- Lorem Ipsum

Product Family Selector Image

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Product Image

### Technical Support

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Product Image

### Licensing

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### Training

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### What's New

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Product Image

### Design Services

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### Quality and Reliability

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### Mature and Discontinued Devices

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# Technical Support

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## Support

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## Answer Database

- Lorem Ipsum

## Submit a Ticket

- Lorem Ipsum

Product Family Selector Image

## Contact Technical Support

[Company Name]
[Address Line 1]
[Address Line 2]
[Country]
[Telephone]
[Fax]
[email address]

## Submit a Support Ticket

### Your Lattice Account

Name

Password

Sign In

Forgot Your Password? I Don't Have an Account?

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# Licensing

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- Mature and Discontinued Devices

### Answer Database
- Lorem Ipsum

### Submit a Ticket
- Lorem Ipsum

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## Narrow Your Results

- Keywords
- Product Family
- Case Type
- Case Category
- Topic

# Answer Database

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## Search Answer Database Only

Search

Group By Product

To sort on a particular column, click on its header label to toggle the sort order between ascending/descending.
Use the Filter pulldown menu in each column to view only records with the selected value in that column.

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## Locations

**North America**

- East
- Midwest
- Texas
- West
- Canada

**North America**

- Austria
- Benelux
- Croatia
- France
- Germany
- India
- Ireland
- Israel
- Italy
- Japan
- Scandinavia
- Switzerland
- United Kingdom

## Answer Database

- Lorem Ipsum

# Design Services

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## Locations

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## Locations

**North America**

- East
- Midwest
- Texas
- West
- Canada

**International**

- Austria
- Benelux
- Croatia
- France
- Germany
- India
- Ireland
- Israel
- Italy
- Japan
- Scandinavia
- Switzerland
- United Kingdom

## Answer Database

- Lorem Ipsum

# [Design Services Location]

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Company Logo

[Company Name]
[Address Line 1]
[Address Line 2]
[Country]
[Telephone]
[Fax]
[email address]

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## Answer Database

- Lorem Ipsum

## Submit a Ticket

- Lorem Ipsum

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# Training

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## Submit a Ticket

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# What's New

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- Lorem Ipsum
- Lorem Ipsum

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- Mature and Discontinued Devices

## Answer Database

- Lorem Ipsum

## Submit a Ticket

- Lorem Ipsum

Product Family Selector Image

# Quality and Reliability

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- Quality and Reliability
- Mature and Discontinued Devices

## Answer Database

- Lorem Ipsum

## Submit a Ticket

- Lorem Ipsum

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# Mature and Discontinued Devices

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## [Device Category]

- Lorem Ipsum
- Lorum Ipsum
- Lorum Ipsum

## [Device Category]

- Lorem Ipsum
- Lorum Ipsum
- Lorum Ipsum

## [Device Category]

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- Lorum Ipsum
- Lorum Ipsum

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Japan
New Zealand
South Korea

**Europe and Africa**
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[Address Line 2]
[Country]
[Telephone]
[Fax]
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## Distributors

Company Logo

[Company Name]
[Address Line 1]
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# FPGA University

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## What is an FPGA Device

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## What is Verilog?

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## What is place and route?

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## How do I get started?

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